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CLAIMS:

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- A dual residue pipelined AD-converter for converting an analog input signal to 1. a digital output signal, said converter comprising a cascade of dual residue converter stages  $(S_1 \dots S_N)$ , the first of said stages  $(S_1)$  comprising means to receive the analog input signal (I), means (G1) to derive one or more digital bits (D1) from said analog input signal and means (H1) to generate first and second residue signals (A1, B1) representing the quantization error left after the AD-conversion of said first stage, each of the following stages (S2 ... SN) in the cascade of dual residue converter stages comprising means to receive the first and second residue signals (A<sub>1</sub> ... A<sub>N-1</sub>, B<sub>1</sub> ... B<sub>N-1</sub>) generated by the previous stage in the cascade, means (G2 ... GN) to derive one or more further digital bits (D2 ... DN) from said received first and second residue signals and each of said following stages except the last one in the cascade comprising means (H<sub>1</sub> ... H<sub>N-1</sub>) to generate first and second residue signals (A<sub>2</sub> ... A<sub>N-1</sub>, B<sub>2</sub> ... B<sub>N-1</sub>) representing the quantization error left after the AD-conversion of the stage, characterized in that each of the stages (S1 ... SN-1) of the dual residue pipelined ADconverter, except the last one, comprises switched capacitor means for the generation of the first and second residue signals  $(A_1 ... A_{N-1}, B_1 ... B_{N-1})$ .
- 2. A dual residue pipelined AD-converter as claimed in claim 1 characterized in that each of said following stages except the last one comprise input capacitors ( $C_3$  ...  $C_6$ ) for receiving during a sampling phase the first and second residue signals generated by the previous stage, switching means ( $\varphi$ ) to transfer during a tracking phase the charge of said input capacitors to first and second output capacitors ( $C_3$ ,  $C_4$ ), and means to generate first and second residue signals ( $A_2$ ,  $B_2$ ) from said first and second output capacitors ( $C_3$ ,  $C_4$ ) respectively.
- 3. A dual residue pipelined AD-converter as claimed in claim 2 characterized in that said switching means (φ) are arranged to transfer charge from said first received residue signal (A<sub>1</sub>) to said first output capacitor (C'<sub>3</sub>) with a gain factor of approximately 2 and charge from both said first (A<sub>1</sub>) and second (B<sub>1</sub>) received residue signals to said second output capacitor (C'<sub>4</sub>) each with a gain factor of approximately 1 in a first sub-range mode

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 $(D_2 = 0)$  and to transfer charge from said second received residue signal  $(B_1)$  to said second output capacitor  $(C'_4)$  with a gain factor of approximately 2 and charge from both said first  $(A_1)$  and second  $(B_1)$  received residue signals to said first output capacitor  $(C'_3)$  each with a gain factor of approximately 1 in a second sub-range mode  $(D_2 = 1)$ .

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- 4. A dual residue pipelined AD-converter as claimed in claim 3 characterized in that said switching means are additionally arranged to transfer charge from both said first  $(A_{1+}, A_{1-})$  and second  $(B_{1+}, B_{1-})$  received residue signals to said first output capacitor  $(2C'_{17})$  with a gain factor of approximately 3/2 and 1/2 respectively and charge from both said first  $(A_{1+}, A_{1-})$  and second  $(B_{1+}, B_{1-})$  received residue signals to said second output capacitor  $(2C'_{18})$  with a gain factor of approximately 1/2 and 3/2 respectively in a third sub-range mode (E=1) which lies symmetrically between said first and second sub-range modes.
- A dual residue pipelined AD-converter as claimed in claim 2 characterized in
  that for the generation of each residue signal (A<sub>2</sub>, B<sub>2</sub>) an operational amplifier (J<sub>3</sub>, J<sub>4</sub>) is provided and that each output capacitor (C'<sub>3</sub>, C'<sub>4</sub>) is connected during the tracking phase (φ) between an output terminal and the inverting input terminal of said operational amplifier.
  - 6. A dual residue pipelined AD-converter as claimed in claim 5 characterized in that one side of each input capacitor  $(2C_{19} \dots C_{30})$  is connected to said inverting input terminal both during the sampling phase  $(\varphi)$  and during the tracking phase  $(\varphi)$  and that each output capacitor  $(C'_{13} \dots C'_{16})$  is charged during the sampling phase by the offset voltage at the inverting input of the operational amplifier  $(J_9, J_{10})$ .
- 7. A dual residue pipelined AD-converter as claimed in any of the preceding claims, characterized in that in that the switched capacitor means are arranged to receive balanced first and second residue signals (A<sub>1+</sub>, A<sub>1-</sub>, B<sub>1+</sub>, B<sub>1-</sub>) and to generate there from balanced first and second residue signals (A<sub>2+</sub>, A<sub>2-</sub>, B<sub>2+</sub>, B<sub>2-</sub>) for application to the next stage in the cascade.